

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) A method, comprising:
receiving a first packet for a buffer in memory;
generating a descriptor indicating a length of the first packet and a buffer address of the buffer;
receiving at least one subsequent packet following the first packet ~~capable of fitting in the buffer with the first packet;~~
determining whether the buffer has available space to store the first packet and the at least one subsequent packet received before transferring the first and the at least one subsequent packet to the buffer;
generating a descriptor for ~~each received~~ the first packet and the at least one subsequent packet indicating the buffer in response to the determining that the buffer has available space;
transferring to the buffer the first packet and the at least one subsequent packet capable of fitting into the buffer in response to the determining that the buffer has available space, wherein the descriptors for the first and the at least one subsequent packet indicate the same buffer while the first and the at least one subsequent packet are stored in the buffer; and
adding the descriptors of the first packet and the at least one subsequent packet written to the buffer to a descriptor array.
2. (Currently Amended) The method of claim 1, wherein in response to receiving one of the at least one subsequent ~~packet~~ packets, further performing:
~~determining whether the buffer has available space for the first packet and the at least one subsequent packet received before transferring to the buffer; and~~
waiting to receive ~~at least~~ one more subsequent packet before transferring the first packet and the received at least one subsequent packet capable of fitting into the buffer to the buffer if the buffer has available space.

3. (Currently Amended) The method of claim 1, wherein the buffer comprises a current buffer, wherein in response to receiving a most recently received packet comprising one recent of the at least one subsequent ~~packet~~ packets not yet transferred to the current buffer, further performing:

determining whether the current buffer has available space for the first packet and the at least one subsequent packet including the ~~recent-subsequent~~ most recently received packet ~~received before transferring~~ not yet transferred to the current buffer, wherein the first packet and ~~the~~ the at least one subsequent packet received between the first packet and the ~~recent-subsequent~~ most recently received packet are transferred in response to determining that that the current buffer does not have available space for the first packet and the at least one subsequent packet including the most recently received not yet transferred to the current buffer ~~recent-subsequent packet~~, and wherein the descriptor generated for the ~~recent-subsequent~~ most recently received packet indicates a next buffer address of a next available buffer in the memory in response to determining that there is not enough available space in the current buffer for the first packet and the at least one subsequent packet including the most recently received packet not yet transferred to the current buffer ~~recent-subsequent packet~~, and wherein the ~~recent-subsequent~~ most recently received packet becomes the first packet for the next available buffer.

4. (Currently Amended) The method of claim 1, wherein the first ~~packets~~ and the at least one ~~received~~ subsequent packets are transferred to the buffer in response to a timer expiring.

5. (Currently Amended) The method of claim 1, wherein all packets in ~~at least one~~ the buffer ~~[[are]]~~ is processed by one processor and wherein packets in different buffers are capable of being processed by different processors.

6. (Currently Amended) The method of claim 1, wherein the descriptor generated for each ~~of the at least one~~ subsequent packet that ~~fits into~~ is transferred to the buffer with the first packet indicates a length of the subsequent packet.

7. (Currently Amended) The method of claim 1, further comprising:
indicating in the descriptor for the first packet a number of packets included in the buffer, including the first packet and the at least one subsequent packet that are transferred to the buffer with the first packet.

8. (Currently Amended) The method of claim 1, wherein writing the first packet and ~~each~~ the at least one subsequent packet comprises transmitting on a bus the first packet and ~~each~~ the at least one subsequent packet capable of fitting into the buffer in a single bus transaction to the buffer.

9. (Original) The method of claim 1, wherein the buffer resides in a host memory, wherein an adapter coupled to the host performs receiving the packets, generating the descriptors, transferring the packets to the buffer, and adding the descriptors to a descriptor array.

10. (Withdrawn) A method, comprising:
accessing a first descriptor referencing a first packet in a buffer and indicating a number of packets in the buffer;
extracting a first packet from the buffer identified in the first descriptor;
accessing at least one subsequent descriptor, where the accessed subsequent descriptor is associated with one subsequent packet indicated in the number of packets, and wherein the subsequent descriptor indicates a length of the associated subsequent packet; and
using each accessed subsequent descriptor to access the associated subsequent packets in the buffer.

11. (Withdrawn) The method of claim 1, wherein the packets are transmitted over a network to an adapter, wherein the adapter generates the descriptors and transfers the packets to buffers in a host memory, and wherein an adapter driver uses the descriptors to access one or more packets from the buffers in the host memory in response to receiving a signal from the adapter that packets are in the host memory.

12. (Currently Amended) A system, comprising:
a memory including a plurality of buffers;
an Input/Output (I/O) device interface in data communication with the memory and
having circuitry enabled to:

[[i]] receive a first packet for a buffer in the memory;

[[ii]] generate a descriptor indicating a length of the first packet and a buffer
address of the buffer;

[[iii]] receive at least one subsequent packet following the first packet ~~capable of
fitting in the buffer with the first packet;~~

determine whether the buffer has available space to store the first packet and the
at least one subsequent packet received before transferring the first and the at least one
subsequent packet to the buffer;

[[iv]] generate a descriptor for ~~each received~~ the first packet and the at least one
subsequent packet indicating the buffer in response to the determining that the buffer has
available space;

[[v]] transfer to the buffer the first packet and the at least one subsequent packet
capable of fitting into the buffer in response to the determining that the buffer has
available space, wherein the descriptors for the first and the at least one subsequent
packet indicate the same buffer while the first and the at least one subsequent packet are;
and

[[vi]] add the descriptors of the first packet and the at least one subsequent
packet written to the buffer to a descriptor array.

13. (Currently Amended) The system of claim 12, wherein in response to receiving
one subsequent packet, the circuitry is further enabled to:

~~determine whether the buffer has available space for the first packet and the at least one
subsequent packet received before transferring to the buffer; and~~

wait to receive at least one more subsequent packet before transferring the first packet
and the received at least one subsequent packet capable of fitting into the buffer to the buffer if
the buffer has available space.

14. (Currently Amended) The system of claim 12, wherein the buffer comprises a current buffer, wherein in response to receiving a most recently received packet comprising one recent of the at least one subsequent packet not yet transferred to the current buffer, wherein the circuitry is further enabled to:

determine whether the current buffer has available space for the first packet and the at least one subsequent packet including the ~~recent-subsequent~~ most recently received packet ~~received before transferring~~ not yet transferred to the current buffer, wherein the first packet and ~~the~~ at least one subsequent packet received between the first packet and the ~~recent-subsequent~~ most recently received packet are transferred in response to determining that that the current buffer does not have available space for the first packet and the at least one subsequent packet including the most recently received not yet transferred to the current buffer ~~recent-subsequent packet~~, and wherein the descriptor generated for the ~~recent-subsequent~~ most recently received packet indicates a next buffer address of a next available buffer in the memory in response to determining that there is not enough available space in the current buffer for the first packet and the at least one subsequent packet including the most recently received not yet transferred to the current buffer ~~recent-subsequent packet~~, and wherein the ~~recent-subsequent~~ most recently received packet becomes the first packet for the next available buffer.

15. (Currently Amended) The system of claim 12, further comprising:
a timer, wherein the first ~~packets~~ packet and ~~received~~ the at least one subsequent ~~packets~~ packet are transferred to the buffer in response to a timer expiring.

16. (Currently Amended) The system of claim 12, further comprising:
a plurality of processors, wherein all packets in ~~[[one]]~~ the buffer ~~[[are]]~~ is processed by one processor and wherein packets in different buffers are capable of being processed by different processors.

17. (Currently Amended) The system of claim 12, wherein the descriptor generated for each of the at least one subsequent packet that ~~fits~~ is transferred into the buffer with the first packet indicates a length of the subsequent packet.

18. (Currently Amended) The system of claim 12, wherein the circuitry is further capable of performing:

indicating in the descriptor for the first packet a number of packets included in the buffer, including the first packet and the at least one subsequent packet that are transferred to the buffer with the first packet.

19. (Currently Amended) The system of claim 12, further comprising:
a bus interfacing the memory and the I/O device interface, wherein the circuitry writes the first packet and ~~each~~ the at least one subsequent packet by transmitting on the bus the first packet and ~~each~~ the at least one subsequent packet capable of fitting into the buffer in a single bus transaction to the buffer.

20. (Currently Amended) The ~~method~~ system of claim ~~[[1]]~~ 12, wherein the I/O device comprises a network adapter.

21. (Withdrawn) A system, comprising:
a memory including a plurality of buffers;
circuitry in data communication with the memory enabled to:
(i) access a first descriptor referencing a first packet in a buffer in the memory and indicating a number of packets in the buffer;
(ii) extract a first packet from the buffer identified in the first descriptor;
(iii) access at least one subsequent descriptor, where the accessed subsequent descriptor is associated with one subsequent packet indicated in the number of packets, and wherein the subsequent descriptor indicates a length of the associated subsequent packet; and
(iv) use each accessed subsequent descriptor to access the associated subsequent packets in the buffer.

22. (Withdrawn) The system of claim 21, wherein the packets are transmitted over a network to an adapter, wherein the adapter generates the descriptors and transfers the packets to buffers in a host memory, and wherein an adapter driver uses the descriptors to access one or

more packets from the buffers in the host memory in response to receiving a signal from the adapter that packets are in the host memory.

23. (Currently Amended) A system in communication with a network, comprising:
a memory including a plurality of buffers;
an adapter in data communication with the network and the memory and having circuitry enabled to:

[[i]] receive a first packet for a buffer in the memory;

[[ii]] generate a descriptor indicating a length of the first packet and a buffer address of the buffer;

[[iii]] receive at least one subsequent packet following the first packet ~~capable of fitting in the buffer with the first packet;~~

determine whether the buffer has available space to store the first packet and the at least one subsequent packet received before transferring the first and the at least one subsequent packet to the buffer;

[[iv]] generate a descriptor for ~~each received~~ the first packet and the at least one subsequent packet indicating the buffer in response to the determining that the buffer has available space;

[[v]] transfer to the buffer the first packet and the at least one subsequent packet capable of fitting into the buffer in response to the determining that the buffer has available space, wherein the descriptors for the first and the at least one subsequent packet indicate the same buffer while the first and the at least one subsequent packet are stored in the buffer; and

[[vi]] add the descriptors of the first packet and the at least one subsequent packet written to the buffer to a descriptor array.

24. (Currently Amended) The system of claim 23, wherein in response to receiving one of the at least one subsequent packet, the circuitry is further enabled to:

~~determine whether the buffer has available space for the first packet and the at least one subsequent packet received before transferring to the buffer; and~~

wait to receive at least one more subsequent packet before transferring the first packet and the received at least one subsequent packet capable of fitting into the buffer to the buffer if the buffer has available space.

25. (Currently Amended) An article of manufacture comprising at least one of a hardware device having hardware logic and a computer readable storage medium having computer executable code enabled to cause operations to:

receive a first packet for a buffer in memory;

generate a descriptor indicating a length of the first packet and a buffer address of the buffer;

receive at least one subsequent packet following the first packet ~~capable of fitting in the buffer with the first packet;~~

determine whether the buffer has available space to store the first packet and the at least one subsequent packet received before transferring the first and the at least one subsequent packet to the buffer;

generate a descriptor for ~~each received~~ the first packet and the at least one subsequent packet indicating the buffer in response to the determining that the buffer has available space;

transfer to the buffer the first packet and the at least one subsequent packet capable of fitting into the buffer in response to the determining that the buffer has available space, wherein the descriptors for the first and the at least one subsequent packet indicate the same buffer while the first and the at least one subsequent packet are stored in the buffer; and

add the descriptors of the first packet and the at least one subsequent packet written to the buffer to a descriptor array.

26. (Currently Amended) The article of manufacture of claim 25, wherein the operations further comprise in response to receiving one of the at least one subsequent packet:

~~determine whether the buffer has available space for the first packet and the at least one subsequent packet received before transferring to the buffer; and~~

wait to receive ~~at least~~ one more subsequent packet before transferring the first packet and the received at least one subsequent packet capable of fitting into the buffer to the buffer if the buffer has available space.

27. (Currently Amended) The article of manufacture of claim 25, wherein the buffer comprises a current buffer, wherein the operations further comprise in response to receiving a most recently received packet comprising one of the at least one subsequent packet not yet transferred to the current buffer:

determine whether the buffer has available space for the first packet and the at least one subsequent packet including the ~~recent-subsequent~~ most recently received packet ~~received before transferring not yet transferred~~ to the current buffer, wherein the first packet and at least one the at least one subsequent packet received between the first packet and the ~~recent-subsequent~~ most recently received packet are transferred in response to determining that that current buffer does not have available space for the first packet and the at least one subsequent packet including the most recently received packet not yet transferred to the current buffer ~~recent-subsequent packet~~, and wherein the descriptor generated for the ~~recent-subsequent~~ most recently received packet indicates a next buffer address of a next available buffer in the memory in response to determining that there is not enough available space in the buffer for the first packet and the at least one subsequent packet including the most recently received not yet transferred to the current buffer ~~recent-subsequent packet~~, and wherein the ~~recent-subsequent~~ most recently received packet becomes the first packet for the next available buffer.

28. (Currently Amended) The article of manufacture of claim 25, wherein the first ~~packets~~ packet and ~~received~~ at least one subsequent ~~packets~~ packet are transferred to the buffer in response to a timer expiring.

29. (Currently Amended) The article of manufacture of claim 25, wherein all packets in ~~at least one~~ the buffer ~~[[are]]~~ is processed by one processor and wherein packets in different buffers are capable of being processed by different processors.

30. (Currently Amended) The article of manufacture of claim 25, wherein the descriptor generated for each of the at least one subsequent packet that ~~fits into~~ is transferred to the buffer with the first packet indicates a length of the subsequent packet.

31. (Currently Amended) The article of manufacture of claim 25, wherein the operations further comprise:

indicate in the descriptor for the first packet a number of packets included in the buffer, including the first packet and the at least one subsequent packet ~~packets~~ that are transferred to the buffer with the first packet.

32. (Currently Amended) The article of manufacture of claim 25, wherein writing the first packet and ~~each~~ the at least one subsequent packet comprises transmitting on a bus the first packet and ~~each~~ the at least one subsequent packet capable of fitting into the buffer in a single bus transaction to the buffer.

33. (Original) The article of manufacture of claim 25, wherein the buffer resides in a host memory, wherein an adapter coupled to the host performs receiving the packets, generating the descriptors, transferring the packets to the buffer, and adding the descriptors to a descriptor array.

34. (Withdrawn) An article of manufacture enabled to cause operations to:
access a first descriptor referencing a first packet in a buffer and indicating a number of packets in the buffer;
extract a first packet from the buffer identified in the first descriptor;
access at least one subsequent descriptor, where the accessed subsequent descriptor is associated with one subsequent packet indicated in the number of packets, and wherein the subsequent descriptor indicates a length of the associated subsequent packet; and
use each accessed subsequent descriptor to access the associated subsequent packets in the buffer.

35. (Withdrawn) The article of manufacture of claim 34, wherein the packets are transmitted over a network to an adapter, wherein the adapter generates the descriptors and transfers the packets to buffers in a host memory, and wherein an adapter driver uses the descriptors to access one or more packets from the buffers in the host memory in response to receiving a signal from the adapter that packets are in the host memory.